Fermilab FERMILAB-PUB-04-427-E D0 DECEMBER 2004

Design of an Upgraded D0 Silicon Microstrip Tracker for Run IIb at the Tevatron

K. Hanagaki *
for the D0 Collaboration
Fermilab, P.O.Box 500, Batavia, IL, 60510

Abstract

The D0 collaboration planned to upgrade the Silicon Tracker to withstand the radiation dose corresponding to above 2 fb^{-1} of data. This new detector was designed to be functional up to at least 15 fb^{-1}. We report on the design of the new Silicon Tracker with details of the innermost layer.

Key words: Silicon Tracker, Flex Printed Circuit Cable
PACS: 29.40.Gx

1 Introduction

The D0 Silicon Microstrip Tracker (SMT) is used to tag a b-jet by looking for a displaced vertex. The present detector is expected to withstand a radiation dose corresponding to 3.5 fb^{-1} with large uncertainty while the Tevatron collider was planning to deliver 15 fb^{-1}. Therefore, D0 collaboration needed to upgrade the SMT to survive while accumulating 15 fb^{-1} of data.

2 Design Overview

The upgraded detector consists of six layers of silicon sensors, divided into two radial groups, as shown in Fig. 1. The inner group, called Layer 0 and 1, is mounted on the integrated support made of carbon fiber. These two layers

* Corresponding author. ph +1-630-840-2327
Email address: kazu@fnal.gov (K. Hanagaki).

are assembled into one unit, extending from 18 mm to 39 mm radially. The outer group, called Layer 2 to 5, uses the stave support structure. This outer group occupies from 53 mm to 164 mm radially. The increase in the number of layers from four in the present detector to six would improve the pattern recognition in the higher instantaneous luminosity. The radius of innermost layer is smaller, and the outermost layer is larger than the present detector (2.7 cm $< R <$ 10 cm). This would facilitate improved impact parameter resolution and momentum resolution. The monte carlo simulation predicts a momentum resolution of 3% and an impact parameter resolution of 15 μm for a 10 GeV/c track.

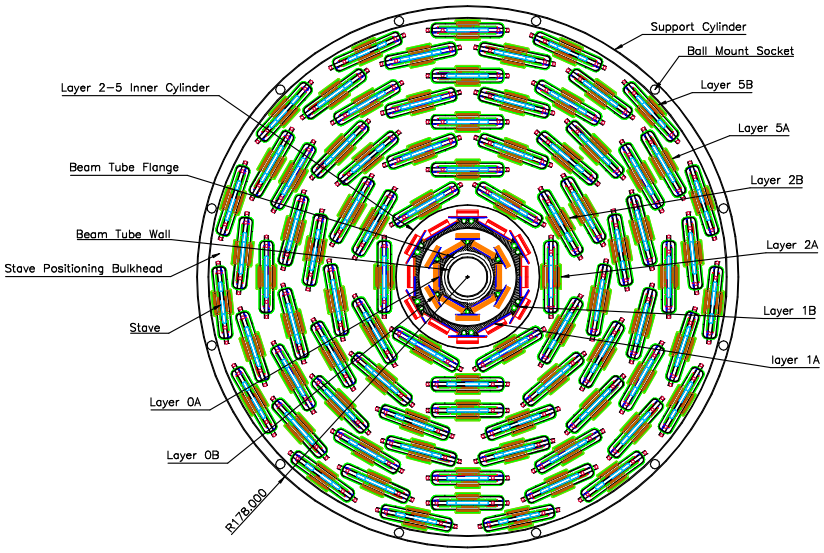

Fig. 1. End view of Layer 0-1 modules, Layer 2-5 staves and the outer silicon-positioning bulkhead.

The upgraded tracker uses only single sided silicon sensors because 1) the emphasis will be oriented to high p_T physics in run IIb, 2) the double sided silicon sensor have limited radiation hardness, and 3) large number of sensor type complicates the production process. There are three types of sensors, two-chip wide for Layer 0, three-chip wide for Layer 1, and five-chip wide for Layers 2-5. They all have only axial strips. The sensor thickness is 320 μm. The Layer 0 and 1 have only axial readout, however, Layer 2 to 5 have both axial and 2° stereo readout realized by rotating the sensors. The silicon sensors are AC-coupled, single-metal p^+ on n-bulk silicon devices with integrated polysilicon resistors. In order to operate at high bias voltage (up to 700 V for Layer 0 and 1, and 350 V for Layers 2-5), a single guard ring structure with a peripheral n-well at the scribing edge has been developed in cooperation with Hamamatsu.

Each silicon sensor is read out by the newly developed SVX4 chip [1]. The SVX4 has been fabricated in 0.25 μm commercial CMOS technology. This

deep submicron technology affords the SVX4 radiation tolerance up to 20 M-rad (roughly equals to 20 fb^{-1} of data accumulation). There are 128 parallel input channels with 48 μm pitch per SVX4 chip. The SVX4 consists of the preamp, the 46 cell pipeline, the 8-bit ADC, and the back-end readout control circuits. A double correlated sampling scheme is used in the analog parts. The shaping time of 113 ns was selected based on the originally planned beam crossing interval of 132 ns. For a constant risetime of 69 ns, the front-end noise was measured to be $41 \times C$ (pF) electrons plus some constant noise (300 to 500 electrons). The digitization (readout) frequency is 106 (53) MHz. The sparsification capability is equipped in the back-end control. The number of readout channels in the upgraded SMT is 950976 in total.

The SVX4 chips are mounted on hybrids produced by thick film printing technology on Beryllia ceramic substrate. The hybrids are directly glued on top of the sensors in Layer 1 to 5. The sensor and SVX4 chip are connected by the wire-bonding. The readout signals and the control signals to the SVX4 are relayed through the low mass jumper cables, junction cards, twisted pair cables, and adapter cards to the present DAQ system. To accommodate the difference between the SVX2 in the present detector and the SVX4, the path from the hybrid to the adapter cards have been newly developed and prototyped. The main differences are the operation voltage (2.5 V for SVX4, and 5 V for SVX2), and the output data driver (differential signals in SVX4, and single ended signals in SVX2). In the Layer 0 there is another cable between the silicon sensor and the hybrid, which will be described in a separate section below.

3 Outer Layers

Each Layer 2-5 module consist of a hybrid which reads out two independent sets of sensors. There are four types of modules, 10 cm and 20 cm long detectors, axial and stereo each. In case of 20 cm detectors, two 10 cm sensors are ganged together by wire-bonding. These Hamamatsu sensors have 60 μm readout pitch and intermediate strips. A few hundreds production sensors have already been delivered. No single device has a leakage current above 400 nA up to 500 V, well within our specification that the junction breakdown voltage be greater than 350 V. This requirement is important to keep the silicon sensor fully depleted as the high radiation dose raises the depletion voltage by type inversion. The hybrid accommodates ten daisy chained SVX4 chips, five to read out each side of the module. It also provides the bias voltage to the silicon sensor with the low pass filtering circuits. Several modules were prototyped to measure basic performance such as noise level. Assuming a minimum ionizing particle creates 22000 electrons in the 320 μm thick silicon sensors, the signal to noise (S/N) ratio was identified to be 16 for 10 cm detector, and

11 for 20 cm detector. The different noise level is attributed to the size of the load capacitance.

Each stave consists of two 10 cm modules and two 20 cm modules, the axial measurement from one side of the carbon fiber core, and the stereo measurement from the other side of the core, and C-channels to provide stiffness. PEEK cooling tubes locate inside the core keep the Layer 2 sensors below $0°C$, and Layer 3-5 sensors below $+5°C$. These staves are mounted on the silicon-positioning membrane and the silicon-positioning bulkhead, both made of carbon fiber reinforced resin, assembled into a barrel unit. The new SMT is divided into two at $z = 0$, there are two barrel units for positive and negative z location. These parts have been prototyped and measured, showing no serious problems.

4 Layer 1

The Layer 1 modules consist of a hybrid glued on top of a 7.9 cm long three-chip wide silicon sensors. The readout pitch of the sensors are 58 μm with intermediate strips. Several sensors have been prototyped by Hamamatsu. The initial tests indicate that the sensors are of good quality. For example, the average strip leakage current has been measured to be 0.4 nA at the full depletion voltage. By building a few prototype modules, the noise level was measured to be 1050 electrons, corresponding to the S/N ratio of 21.

Each Layer 1 module is directly mounted on a castellated carbon fiber structure, six modules along z direction in a phi sector. There are two units again divided at $z = 0$. The cooling tubes are placed between the castellated structure and the inner support made of carbon fiber. The silicon sensor must be maintained below $-5°C$. Assuming 0.5 W per chip [1] and 0.1 W per sensor of heat generation, this requires the temperature of the coolant to be $-15°C$ with a flow rate of 0.1 m/s. The coolant is 40% ethylene glycol in water mixture.

5 Layer 0 Design

In Layer 0 or L0, the space constraints, the cooling issue of the silicon sensor, and the amout of material require us to transmit the analog signal from the sensor to the SVX4 readout chip, which is mounted outside the fiducial region along the beam direction [2]. We use a flexible printed circuit cable for the

[1] The actual power consumption was measured to be 0.3 W. Thus the 0.5 W heat load is conservative.

readout, referred to as the analog cable. The maximum cable length is 46.4 cm. There are two serious issues related to the noise caused by the analog cable. The first is front-end noise of the readout chip due to the large capacitive load. The second is pick-up noise by the analog cable, as the current CDF experience for L00 indicates [3].

Single unit of L0 module consists of a 7.9 cm long 50 μm readout pitch silicon sensor, two analog cables with constant 91 μm pitch, and a two-chip hybrid. The low-pass filter board for the bias is glued on top of the sensor. The two analog cables are laminated together with the shift by 45.5 μm to achieve an effective pitch of 45.5 μm. Each cable has 128 plus one spare signal traces, and two traces for biasing the sensor and its return. Signal traces are 16 μm wide gold-plated copper on the Kapton substrate, fabricated by plasma etching technology widely used in the printed circuit. Because of the requirements of radiation hardness and fire safety regulations at Fermilab, Kapton type polyimide is the only possible choice for the substrate of the analog cable. The prototype cables were successfully produced by Dyconex in Switzerland [4] with 100% yield in the last batches. The capacitance of one trace to the rest of the traces was measured to be 0.35 pF/cm. This is below the requirement of <0.5 pF/cm which is the upper limit to achieve the design goal of S/N ratio better than 10 after 15 fb^{-1}. In order to avoid capacitance increase contributed from the neighboring analog cables, Kapton based spacers with large air volume was expected to be placed between each cable. Each L0 module is mounted directly on the carbon fiber structures in a very similar way as Layer 1.

6 Layer 0 Noise Study

Having a well defined grounding plane is crucial to reduce the pick-up noise for L0. Without such a grounding plane, the analog cable actually picks up RF like an antenna. The noise level depends almost linearly on the non-shielded area around the cable. In our proposed scheme, both the sensor's and hybrid's ground are tied together to the reference grounding plane. It was found that a low inductance ground connection is very important to suppress pick-up noise. Figure 2, for example, shows the noise level defined as the RMS of the pedestal distribution as a function of the number of wires added to the grounding path from the hybrid in an L0 module prototype and the reference grounding plane. Each wire has the resistance far below 1 Ω, while the total resistance from the hybrid to the grounding plane is a few Ohm. Therefore, the variation of noise level is affected mostly by the inductance. Since the impedance generates potential difference and thus is the noise source, this observation implies that the total impedance is dominated by inductance in our operation frequency range, not by the resistance. By achieving a low inductance grounding connection,

the S/N ratio becomes 11 which is the design goal prior to irradiation.

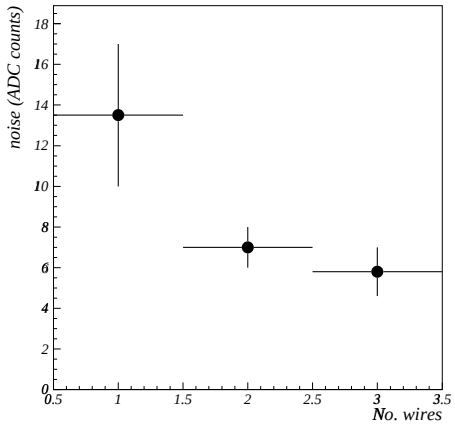

Fig. 2. The noise level vs the number of wires connecting the hybrid and the reference ground plane.

Noise pick-up could come from capacitive coupling to anything. Figure 3 shows the noise level as a function of the distance between the signal traces on the analog cable to the reference grounding plane. Noise pick-up by capacitive coupling is clearly seen. Based on this plot, 500 μm thick spacer was planned to place between the reference grounding plane and the analog cables.

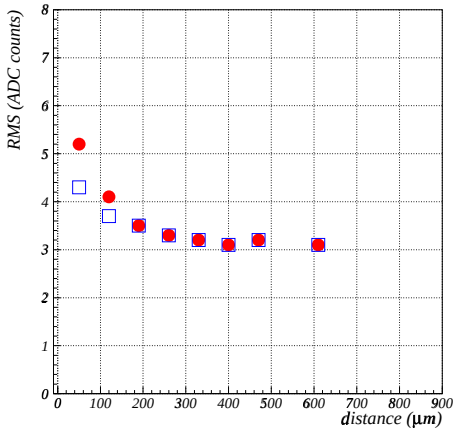

Fig. 3. The noise level vs the distance between the signal trace on the analog cable to the reference grounding plane. The total noise is shown by circles (red), and the differential noise by open squares (blue).

Because the carbon fiber is the direct support of L0 modules, the electrical properties of carbon fiber was mapped [5] to design a proper grounding scheme. The main conclusion is that the carbon fiber is a good conductor for high frequency AC, such as 10MHz, which is relevant for us. At that frequency

there is no distinction among copper, stainless steel, and carbon fiber. This result implies that carbon fiber must be treated as a conductor and can be used as a reference grounding plane if it is properly grounded. The basic idea is to have all the carbon fiber components electrically connected to the detector ground. This would be established by co-curing Kapton flex circuits into the carbon fiber, where the exposed copper traces on the flex circuits are facing the carbon fiber. These co-cured circuits have gold-plated pads for electrical connections. Then the silicon sensor and the hybrid (or SVX4) grounds are tied to the carbon fiber structures via the gold-pated pads on the co-cured circuits. The paths from the hybrid/SVX4 to the gold-plated pads are routed by other Kapton flex circuits with the shortest path to achieve a low inductance connection.

7 Conclusions

The design of D0 SMT for run IIb was finalized. The project had prototyped all components of the design, and found no serious technical issues. Reliable analog cables were designed and successfully fabricated. We found the importance of low inductance ground connection for L0 and developed a method to achieve such a ground connection by the application of the carbon fiber support structure.

Acknowledgment

I am grateful to the D0 Run IIb silicon tracker group.

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